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# Nanoscale patterning of electronic devices at the amorphous $\text{LaAlO}_3/\text{SrTiO}_3$ oxide interface using an electron sensitive polymer mask

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# Nanoscale patterning of electronic devices at the amorphous $\text{LaAlO}_3/\text{SrTiO}_3$ oxide interface using an electron sensitive polymer mask

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A simple approach is presented for designing complex oxide mesoscopic electronic devices based on the conducting interfaces of room temperature grown  $\text{LaAlO}_3/\text{SrTiO}_3$  heterostructures. The technique is based entirely on methods known from conventional semiconductor processing technology, and we demonstrate a lateral resolution of  $\sim 100$  nm. We study the low temperature transport properties of nanoscale wires and demonstrate the feasibility of the technique for defining in-plane gates allowing local control of the electrostatic environment in mesoscopic devices. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>). <https://doi.org/10.1063/1.5026362>

Since the discovery of a two-dimensional conducting electron system (2DES) at the interface between  $\text{TiO}_2$  terminated strontium titanate (STO) and lanthanum aluminate (LAO),<sup>1</sup> the efforts towards exploring, understanding, and utilizing the electronic properties of oxide interfaces have attracted significant attention from all branches of physics and materials science. One example is the drive towards the integration of oxide interfaces in mesoscopic devices to complement the semiconductor heterostructures and bottom-up grown nanostructures which have been the material platform for two decades of research in quantum transport. The oxide electron systems share the properties of low dimensionality and electrostatic gateability<sup>2</sup> with the conventional semiconductor systems but in addition display a wide range of phenomena such as gate-tunable superconductivity, ferroelectricity, magnetism, and spin-orbit coupling caused by strong electron-electron and electron-lattice interactions in regimes not accessible in semiconductors.<sup>3,4</sup> However, the oxide 2DES is highly sensitive to the quality of the epitaxial interfaces and subsequent surface processing,<sup>5,6</sup> and a range of specialized fabrication techniques have therefore been developed for realizing patterned oxide devices while protecting interfaces and limiting post processing. Such techniques range from patterned growth of the oxide top-layer by hard-mask techniques,<sup>6–10</sup> ion irradiation,<sup>11</sup> thickness variations of the top layer,<sup>12</sup> or the creation of conducting nanostructures using scanning probe lithography.<sup>13</sup> Such approaches are more involved than conventional semiconductor processing and often include wet etching which is difficult to control leading to limited reproducibility and resolution.

Most studies so far have considered crystalline STO-based heterostructures where the top-films are deposited at temperatures above  $\sim 600$  °C. Room temperature (RT) deposition such as for the amorphous LAO/STO (a-LAO/STO) system also leads to conducting interfaces where electrons predominately originate from oxygen vacancies<sup>14,15</sup> and

usually exhibit reduced mobilities compared to crystalline LAO/STO.<sup>16</sup> The key properties of gate-tunability and gate-tunable superconductivity,<sup>17,18</sup> however, remain intact, and moreover, the highest transition temperature reported for the STO-based 2DES was achieved in the a-LAO/STO system.<sup>19</sup> Also, recently, studies were performed on the transport properties of negative- $U$  quantum dot devices which were fabricated from a-LAO/STO heterostructures.<sup>17,20</sup> Thus, the a-LAO/STO system provides an interesting system for mesoscopic oxide devices, and here, we demonstrate that the reduced deposition temperature allows patterning of the interface conductivity by a conventional electron-beam or optical lithography with only minor adjustments. We explore the limitations of the technique in terms of lateral resolution and the performance of nanoscale devices at low temperatures.

Our fabrication procedure is schematically illustrated in Fig. 1(a). The starting point is a (001) STO single crystal with a  $\text{TiO}_2$  terminated surface<sup>21</sup> achieved by first sonicating in ethanol and acetone at room temperature (RT) for 300 s, then for 20 min in deionized (DI) water at 70 °C, and 20 min in *aqua regia* (3:1:16 HCl:HNO<sub>3</sub>:H<sub>2</sub>O) at 70 °C. Finally, following a brief 30 s cleaning in DI water, the substrates are annealed for 60 min at 1000 °C in a tube furnace under oxygen flow and cooled to RT with a ramp rate of 100 °C/h. Substrates for e-beam(optical) lithography are then spin-coated with 2% polymethyl methacrylate (PMMA) diluted in anisole(AZ1505 photo resist) and heated for 1 min at 185 °C(115 °C) on a hot plate. Additionally, the e-beam substrates are spin-coated with a layer of SX-AR-PC 5000 e-spacer, which is heated for 60 s at 115 °C, to reduce distortion during exposure. PMMA(AZ1505) was exposed using standard parameters and the patterns developed in 1:3 Methyl-Isobutyl-Ketone and Isopropanol(MF-321 developer). Before growing the top-layer, the substrates were carefully cleaned in an oxygen plasma for 120 s (calibrated to remove 8 nm of PMMA) and cleaned in Milli-Q (MQ) water for 120 s at RT. Lift-off patterning of a-LAO combined with subsequent high

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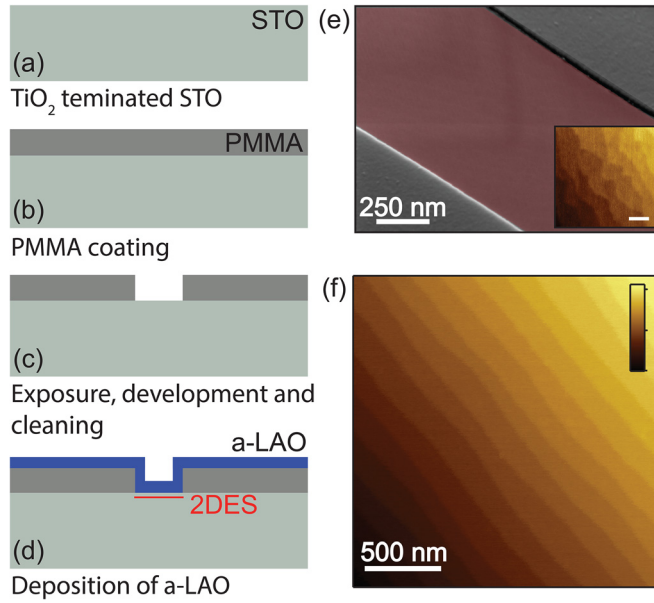


FIG. 1. Schematic illustration of the patterning technique. (a) An STO substrate is prepared with a TiO<sub>2</sub> surface termination. (b) The surface is spin coated in polymer-based electron or optically sensitive resist and (c) conventional techniques are used for exposure and development, followed by careful cleaning. (d) Amorphous LAO is deposited on the substrate by room temperature PLD. (e) SEM image of a 2 μm wide channel taken with a 50° angle to the plane of the substrate. The inset shows an AFM image of the a-LAO/STO. The scale bar is 200 nm. (f) Typical AFM image of the STO surface after cleaning; the color scale is 0–8.5 nm.

temperature annealing and deposition has previously been used for defining insulating structures in crystalline LAO/STO devices.<sup>7</sup> For defining conducting structures, it is, however, crucial that the exposed surface does not contain any resist residues and previous attempts excluding the last cleaning steps have been found to lead to insulating samples.<sup>6</sup> We have tested the patterning technique for both e-beam lithography and optical lithography yielding similar results; in the following, we present the results obtained using the former technique. The final PMMA resist profile is shown in Fig. 1(e), and a representative AFM image of the surface terraces in the exposed channel is shown in Fig. 1(f) after the cleaning procedure. No discernible differences to the as-treated surface are observed. A top layer of 12 nm a-LAO was grown by room temperature Pulsed-Laser-Deposition (PLD).<sup>6</sup> To investigate the properties of the 2DES induced at the exposed interfaces and the spatial resolution of the lithographical patterning, standard Hall-bars (Fig. 2) were defined as well as structures allowing 4-terminal measurements of leakage currents between parallel wires with varying separations [Fig. 3(a)] and of the conductance of wires of varying widths [Fig. 3(c)].

Hall-bar samples were fabricated with a width of  $W = 30 \mu\text{m}$  and a length of  $L = 500 \mu\text{m}$ , and Fig. 2(a) shows a representative sample after the growth of the top layer. Measurements were performed in a dilution refrigerator with a  $\sim 20$  mK base temperature, and standard lock-in techniques ( $\sim 20$  nA current excitation) were used to measure the longitudinal  $V_{xx}$  and transverse  $V_{xy}$  voltage drops as indicated in the figure. The samples were mounted in a sample carrier using conductive silver epoxy, and the overall carrier density was modulated by biasing the conducting back-plane of the sample ( $V_{BG}$ ). No leakage was measured between neighboring Hall-bars

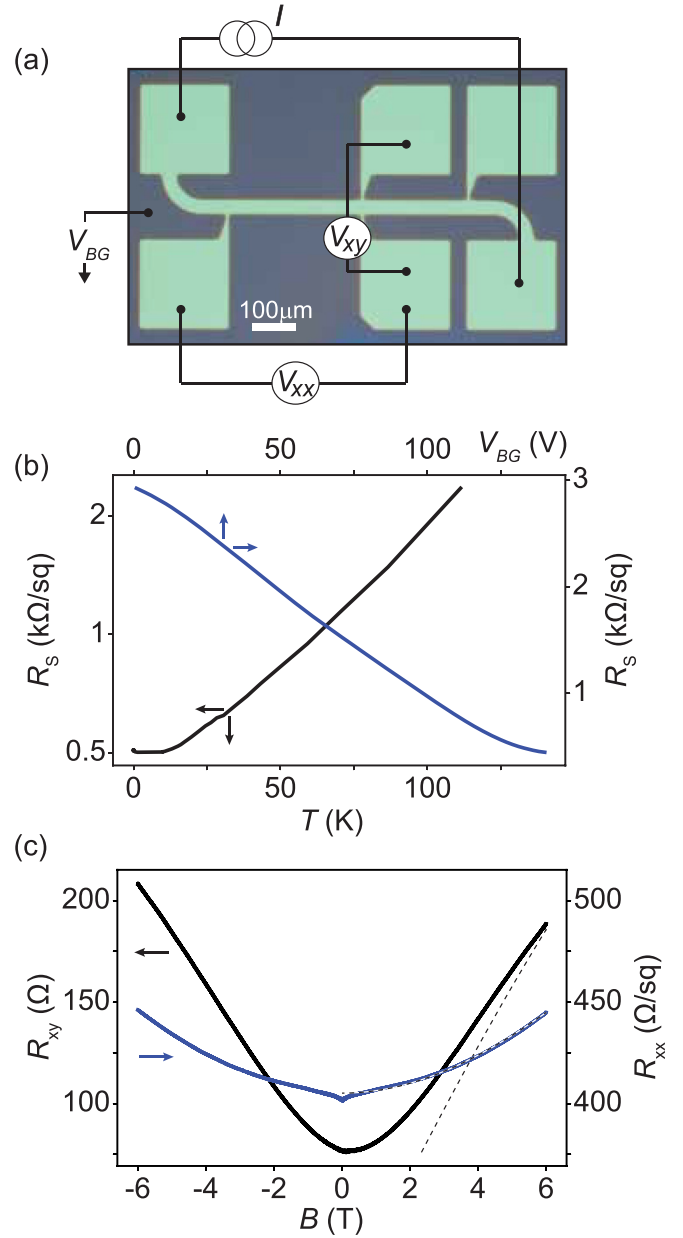


FIG. 2. (a) Optical microscopy image and schematic measurement setup for a typical sample used for Hall characterization. (b) Temperature (black) and back-gate (blue) dependence of the sheet resistance. The cooldown curve shows typical metallic behavior, while the back-gate dependency shows similar behavior to an  $n$ -type semiconductor. (c) Low temperature Hall characterization with  $R_{xy}$  (black) and  $R_{xx}$  (blue) and fits to a two-band model (dashed lines).

on the samples. As seen in Fig. 2(b), the sheet resistance  $R_s = (W/L)V_{xx}/I$  decreases upon cooling as typically observed for metallic oxide interfaces. The dependence of  $R_{xx}$  and  $R_{xy}$  on a perpendicular magnetic field  $B$  at 20 mK is shown in Fig. 2(c). The positive magneto-resistance in  $R_{xx}$  is observed in all samples and has also been reported previously for oxide interfaces and has been attributed to contributions from more than one carrier type.<sup>22,23</sup> The finite value for  $R_{xy}$  at  $B = 0$  is attributed to a contribution from the longitudinal voltage drop due to an off-set of the voltage probes or a non-isotropic current path in the sample. Fitting  $R_{xx}$  and the high-field value of  $R_{xy}$  to the two-band model<sup>24</sup> as shown in the figure, we find a higher density  $n_1 = 4.75 \times 10^{13} \text{ cm}^{-2}$  of low mobility  $\mu_1 = 125 \text{ cm}^2/\text{Vs}$  and a lower density  $n_2 = 7.5 \times 10^{12} \text{ cm}^{-2}$  of high mobility carriers

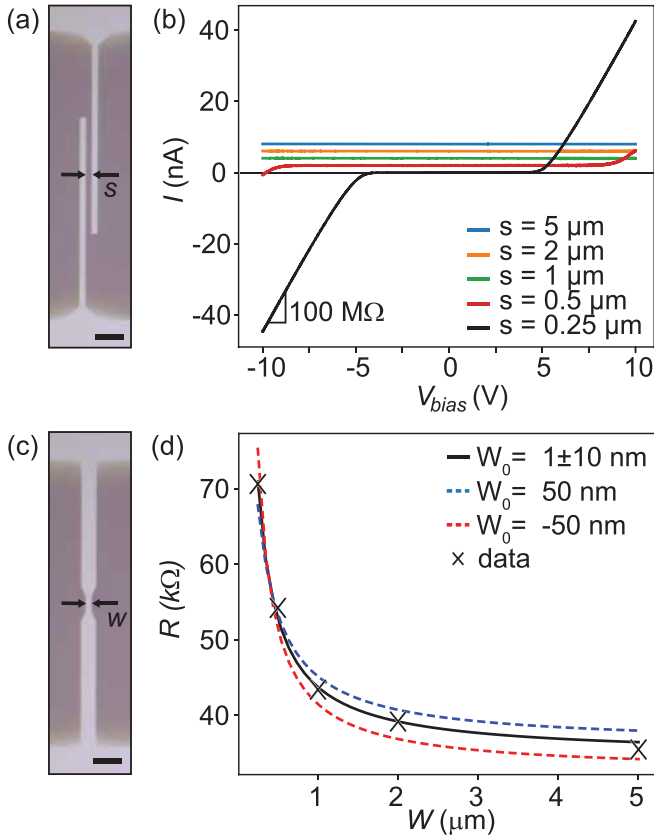


FIG. 3. (a) Optical image of the device used to characterize leakage between closely spaced conducting wires. The scale bar is  $10\ \mu\text{m}$ . (b) Corresponding room temperature IV characteristics of devices with different separations, offset for clarity. No devices show leakage at low bias, and only for the two closest spacings of  $250\ \text{nm}$  and  $500\ \text{nm}$  leakage is observed at  $V_{\text{bias}} \sim 4.5\ \text{V}$  and  $V_{\text{bias}} \sim 9\ \text{V}$ , respectively. (c) Optical image of the device consisting of a central wire with width  $W$ , and the scale bar is  $10\ \mu\text{m}$ . (d) Linear 4-terminal resistance vs.  $W$  at RT for devices each consisting of 5 identical wires in the geometry of (c). The lines show fits to simple geometric relations (see the text).

$\mu_2 = 10\mu_1 = 1250\ \text{cm}^2/\text{V s}$ . These carrier densities are in good agreement with previous studies of the a-LAO/STO system.<sup>15,22</sup> This indicates that the patterning process, in particular, the oxygen plasma cleaning of the STO surface, has no significant consequences for the quality of the 2DES.

As is common for LAO/STO samples, we find that electrostatic gating irreversibly changes the oxide 2DES<sup>25</sup> and the initial measurements [Figs. 2(b) and 2(c)] were performed after cooldown before applying a gate voltage. Figure 2(b) (blue) shows the effect of  $V_{\text{BG}}$ . The sample acts as an  $n$ -type semiconductor, and resistance drops upon increasing  $V_{\text{BG}}$ . No measurable leakage current between back-gate and Hall-bar was observed during these measurements. We note that none of the substrates turned superconducting at low temperature. We do not suspect that this is a consequence of the patterning technique employed here since hard-mask devices were fabricated at the same time using the same batches of substrates without showing superconductivity either, although samples made by the latter technique and measured under the same conditions have previously exhibited superconductivity.<sup>19</sup> Also, even in unpatterned growths, we find significant growth-to-growth variations when substrates exhibit superconductivity. The underlying reason for this variation remains unknown. In total, 18 Hall-bar devices were fabricated on 3 substrates (6 patterned

using PMMA and the rest by optical lithography) of which 12 have been measured displaying the same behavior. In none of the studied devices, we have observed inter-device leakage or substrate leakage induced by the processing. In all, the results of Fig. 2 show that devices patterned on a large scale using the PMMA as a direct mask have the same properties as those made using alternative patterning approaches.

The spatial resolution of the patterning technique is crucial for fabrication of nanoscale devices. The pattern in the PMMA resist can routinely be defined with a resolution below  $50\ \text{nm}$ . The conducting interface is, however, not created until the deposition of the LAO top film in the exposed regions, and depending on the ability of the plasma cleaning step described above and of the plasma of the PLD to enter nanoscale patterns in the  $\sim 100\ \text{nm}$  thick mask layer [Fig. 1(b)], the resulting conducting areas may be smaller than the resist openings. On the other hand, since the interface conductivity is presumably a result of oxygen vacancies created when depositing the top-layer, and that the oxygen diffusion length may be significant, this could lead to conducting regions extending beyond the resist openings. This could be the consequence of under-cut in the exposed resist profile due to exposure by electrons back-scattered from the substrate which is often the case. Thus, in the case where either of these mechanisms are significant, the actual resolution would not be set by the resolution of the lithography. To investigate this, two types of devices were fabricated allowing 4-terminal measurements of (1) the leakage currents between sets of parallel wires with varying separations,  $s = 5, 2, 1, 0.5, 0.25\ \mu\text{m}$ , between the resist openings [Fig. 3(a)] and (2) the conductance of wires defined with varying widths,  $W = 5, 2, 1, 0.5, 0.25\ \mu\text{m}$  [Fig. 3(c)].

Considering first the leakage between separated structures, none of the devices showed leakage at low bias and the three largest wire separations show negligible leak currents up to a bias voltage of  $|V_{\text{bias}}| = 10\ \text{V}$  at room temperature. For the wires separated by  $250\ \text{nm}$  and  $500\ \text{nm}$ , however, a leak current is observed for an applied bias of  $|V_{\text{bias}}| \sim 4.5\ \text{V}$  for the  $250\ \text{nm}$  wire and at  $|V_{\text{bias}}| \sim 9\ \text{V}$  for  $500\ \text{nm}$ . Note that after the devices leak, the currents in Fig. 3(b) are set by a  $100\ \text{M}\Omega$  series resistor included for protection. At low temperatures, the leakage threshold decreased to  $|V_{\text{bias}}| \sim 150\ \text{mV}$  for the smallest separations probably due to the temperature dependent dielectric properties of STO (see below). For all devices, the observed leakage was reversible, suggesting the origin to be a tunneling effect between the parallel wires rather than the electronic discharge or physical rearrangement of atoms in the sample. From AFM inspection of the resist profiles, the edges of the openings have a roughness of about  $25\ \text{nm}$ , and since the measured leakage will be dominated by the points of smallest separation, the absence of leakage at low bias shows that the conducting region extends at most  $100\ \text{nm}$  beyond the resist openings and presumably much less.

Figure 3(d) shows the RT resistance of the wire devices as a function of the width. To reduce the effects of inhomogeneities, each device consists of 5 identical wires in parallel. Each wire is  $100\ \mu\text{m}$  long and has two  $45\ \mu\text{m}$  long sections that are kept at a width of  $5\ \mu\text{m}$  joined together by a central narrow section of length  $L$  and varying width  $W$ . In



the simplest case, we expect the resistance to follow  $R = [L/(W + W_0) + 19]R_S$ , where  $R_S$  is the sheet resistance of the 2DES and  $W_0$  is a possible deviation in the actual width of the conducting area from the width defined in the mask layer. The second term accounts for the resistance of the two wide sections (each with an aspect ratio of 9.5) connected to the central narrow wire. The blue and red traces in Fig. 3(d) show fits to this expression with  $W_0$  fixed at 50 nm and  $-50$  nm, respectively, which does not appropriately describe the data. The black trace, on the other hand, shows a fit including  $W_0$  as a fit parameter, providing an excellent fit to the data with a sheet resistance of  $R_S = 1.8 \pm 0.03 \text{ k}\Omega/\square$  and  $W_0 = 1 \pm 10 \text{ nm}$ . Thus, within the experimental accuracy, the width of the conducting region is consistent with the width of the resist openings even for the most narrow wires. To summarize, the results in Fig. 3 show that within an uncertainty of about 25 nm (given by the roughness of the resist openings defined by the lithography), the conducting regions in the interface reproduce the lithographically defined openings in the resist mask.

Local electrostatic control is an important element in most mesoscopic devices such as quantum dots and quantum point contacts (QPCs). Local gates are usually defined by capacitively coupled metallic top electrodes isolated from the electron system by an oxide. Alternatively, to avoid possible damage due to processing on the samples after the growth of the top-layer, either metallic gates can be used as a part of the mask structure<sup>17</sup> or nearby regions of the 2DES itself can be utilized for gating.<sup>20,26</sup> Figure 4 demonstrates the latter approach using

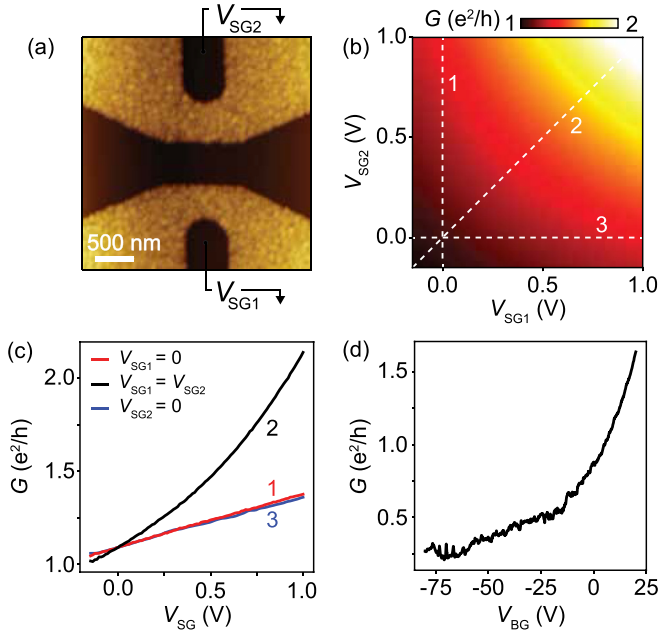


FIG. 4. (a) AFM image of the device consisting of central channels and in-plane side-gates. Channel width, side-gate width, and spacing between the gate and the channel were designed to be 500 nm. (b) 2D plot displaying the effect of each gate on the conductance of the channel within the maximum range of no leak from the side gates. The two side-gates show comparable individual effects on the 2DES with the ability combined to modulate the conductance from 1 to 2  $e^2/h$ . (c) Gate cut-outs corresponding to the dashed lines in (b). The two side-gates modulate the conductance almost identically when operated separately with a much larger effect when operated symmetrically. (d) Back-gate dependence on the conductance. The reduction in gate-efficiency with lower voltage can be explained by the  $E$ -field dependence of the dielectric constant in STO.

the PMMA as the patterning mask for defining a 500 nm wide channel with nearby 2DES side-gates as shown in Fig. 1(a).<sup>26</sup> The separation between the gates and the channel was likewise 500 nm. The conductance of the devices as a function of the voltage  $V_{SG}$  applied to the side-gates and back-gate is shown in Figs. 4(b)–4(d) for a temperature of 20 mK. An interesting regime is that close to pinch-off where only a few channels contribute to the transport, phenomena such as quantized conductance are expected. For all three gates, the conductance significantly decreases with lowering gate potential as the channel is depleted of carriers and the effect of the two side gates is remarkably symmetric. The gate-efficiency, however, progressively decreases at lower gate voltage due to the field dependent dielectric constant of STO,<sup>26</sup> and the side-gates could be operated without leakage only within the range of  $[-0.15 \text{ V}, 1 \text{ V}]$ . A similar device with lower dimensionality was fabricated after these measurements. Here, conductance was observed through a 100 nm channel with a non-leaking interval of  $[-0.15 \text{ V}, 0.15 \text{ V}]$  and similar results from the transport measurements. Although the devices were operated in the regime close to pinch-off, no quantization of conductance nor signatures of conductance fluctuation were observed. This is similar to previous reports<sup>27</sup> and is interpreted as a current carried by many weakly transmitting transverse modes. Systematic investigations of device geometries varying the potential steepness around the channel may shed further light on this.

In conclusion, we have presented a patterning approach for the fabrication of mesoscopic devices from STO-based heterostructures with room temperature grown top-layers. The technique utilizes only conventional polymer resists sensitive to either electron or optical exposure and allows for patterning with a resolution of at least 100 nm without affecting the quality of the 2DES. Finally, we demonstrated devices implementing local electrostatic gate-control of the carrier density in narrow constrictions. Various aspects of the patterning approach were demonstrated using room temperature grown amorphous LAO as the top-layer; however, alternative STO-based conducting room temperature grown interfaces have been reported,<sup>16,18</sup> and we expect that the techniques reported in this study may be directly applied to such systems as well. The results present a simple way to bridge the gap between oxide-based quantum device fabrication and state-of-the-art semiconductor processing.

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